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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/082,500 | 02/25/2002 | Cheng-Lien Chiang | BDG005-3 | 3761 |

7590 12/15/2003

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| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 12/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/082,500 | CHIANG, CHENG-LIEN | |
| | Examiner | Art Unit | |
| | Chris C. Chu | 2815 | AW |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Peri d for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 August 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 - 150* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *31 - 60, 121 - 140 and 146 - 150* is/are allowed.

6)☒ Claim(s) *See Continuation Sheet* is/are rejected.

7)☒ Claim(s) *See Continuation Sheet* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Continuation of Disposition of Claims: Claims rejected are 1 - 13, 15 - 30, 61 - 63, 65, 66, 68, 70, 71, 73, 75 - 78, 80, 81, 83, 85, 86, 88, 90, 91, 93, 95, 96, 98, 100, 101, 103, 105, 106, 108, 110, 111, 113, 115, 116, 118, 120, 141 - 143 and 145.
Continuation of Disposition of Claims: Claims objected to are 14,64,67,69,72,74,79,82,84,87,89,92,94,97,99,102,104,107,109,112,114,117,119 and 144.

## DETAILED ACTION

### *Response to Appeal Brief*

1. In view of the appeal brief filed on August 21, 2003, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

### *Petition*

2. Applicant has filed on August 21, 2003 five petitions under 37 C.F.R. § 1.181. relating to various objections to the drawings and specification. Each of these petitions has been granted. Accordingly:

- The drawing Objection for a missing feature in claims 3, 11 and 22 under 37 C.F.R. § 1.83(a) has been withdrawn.
- The drawing Objection for a missing feature in claims 16, 26, 36 and 46 under 37 C.F.R. § 1.83(a) has been withdrawn.

- The drawing Objection for a missing feature, specifically the limitation "a conductive trace that extends through an opening in the first housing portion," in claim 11 under 37 C.F.R. § 1.83(a) has been withdrawn.
- The drawing Objection for improper reference characters under 37 C.F.R. § 1.84(p)(4) has been withdrawn.
- The specification Objection for lack of brief description of Figs. 1 A - 14B has been withdrawn.

***Drawings/Specification***

3. The drawings and specification are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "144" has been used to designate both a "photoresist layer" (e.g. Figs 2C - 2F and associated portion of the specification on page 10) and alternatively, a "metal trace" (e.g. Figs. 3C - 14 and page 11 of the specification). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3 - 9, 21, 23 - 29, 61, 63, 66, 68, 71, 73, 91, 93, 96, 98, 101, 103, 106, 108, 111, 113, 116 and 118 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamanaka '723.

a. Yamanaka discloses in Figs. IA - 3, column 3, line 66 - column 4, line 14, column 6, lines 3 - 10 and column 7, lines 14 – 19:

- a semiconductor chip (7) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces (e.g. claims 61, 66, and 71), wherein the upper surface includes a light sensitive cell (column 7, lines 14 -19) and a conductive pad (between the chip and a wire 8).

b. Regarding e.g. claims 1, 3 - 5 and 61, Yamanaka discloses in Figs. IA - 3, column 3, line 66 - column 4, line 14, column 6, lines 3 - 10 and column 7, lines 14 - 19 an optoelectronic semiconductor package device, comprising:

- an insulative housing (5 and 9) that includes a first single-piece non-transparent insulative housing portion (5) that contacts the chip, covers the lower surface and the side surface (e.g. claims 61, 66 and 71) and is spaced from the light sensitive cell as well as the upper surface (e.g. claims 3 and 11) and a second transparent insulative housing portion (9 or 9 & 91) that contacts the first housing portion, the conductive

trace (e.g. claim 4) as well as the light sensitive cell and is spaced from the lower surface of the chip by adhesive spacer (element 71, e.g. claims 5, 11 and 61), wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within the peripheral ledge (e.g. claims 1 and 13) and is exposed; and

- a conductive trace (3) that extends through an opening in the first housing portion (e.g. claim 61) and is electrically connected to the pad inside the insulative housing.

i. Regarding e.g. claims 6, 24, 63, 68, 73, 93, 98, 103, 108, 113 and 118, Yamanaka discloses in Figs. 1 A – 3 the first housing portion including a peripheral ledge that forms a peripheral portion of the top surface, and the second housing portion (9) being located within and recessed relative to the peripheral ledge.

ii. Regarding e.g. claims 7 and 25, Yamanaka discloses in Figs. 1 A - 3, column 3, line 66 - column 4 and line 14, column 6, lines 3 - 10 the first housing portion being a transfer molded material that includes a peripheral ledge, and the second housing portion being a cured polymeric material that is located within the peripheral ledge and includes a first surface (the portion that covers the top of chip 7) that faces towards the chip and contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that faces away from the chip and provides the central portion of the top surface and is exposed.

iii. Regarding e.g. claims 8 and 28, Yamanaka discloses in Figs. 1 A - 3 the conductive trace extending through a peripheral side surface of the first housing portion and contacting the second housing portion without

extending through a surface of the second housing portion. Furthermore, the term "a surface" (last line of claim) reads on at least one surface through which the conductive trace doesn't extend. In Yamanaka, the conductive trace doesn't extend through at least the top surface.

iv. Regarding e.g. claims 9 and 29, Yamanaka discloses in Figs. 1A - 3 the device being devoid of an electrical conductor that extends through opposing surfaces of the second housing portion. The examiner reads the term "electrical conductor" as referring to an additional structure, separate from the conductive trace, because if the term "electrical conductor" were to read on the "conductive trace", the claim would raise 112-1st new matter issues.

v. Regarding e.g. claims 66 and 71, Yamanaka discloses in Figs. 1A - 3 that the optoelectronic semiconductor package device further comprises the conductive trace being bent outside the insulative housing (e.g. claim 66) and does not contact an insulative material outside the first housing portion (e.g. claim 71).

c. Regarding claims 21 and 23, Yamanaka also discloses in Figs. IA - 3, column 3, line 66 - column 4, line 14, column 6, lines 3 - 10 and column 7, lines 14 - 19 that the device also comprises:

- an insulative housing (5 and 9) that includes a top surface, a bottom surface and uncurved peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first (5) and second (9) insulative housing portions, the first housing portion is a single-piece that

provides the bottom surface and is non-transparent, and the second housing portion contacts the upper surface, the light sensitive cell and the conductive trace (3) is spaced from the lower surface of the chip (e.g. claim 23), is farther from the bottom surface of the insulative housing than the lower surface of the chip is from the bottom surface, provides at least a portion of the top surface of the insulative housing and is transparent; and

- a conductive trace (3) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

i. Regarding e.g. claim 26, Yamanaka discloses in Figs. 1A - 3 that the insulative housing consists of the first and second housing portions.

ii. Regarding claim 27, Yamanaka discloses in Figs. 1A- 3 the light sensitive cell contacting a major surface of the second housing portion that faces towards and being parallel to the upper surface.

d. Regarding claims 91, 96, 101, 106, 111 and 116, Yamanaka also discloses that the device further comprises:

- an insulative housing (5 and 9) that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first (5) and second (9) insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers and contacts the lower surface, and covers (as opposed to "contacts") the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light

sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the central portion of the top surface is recessed relative to the peripheral portion of the top surface (e.g. claim 101), the top surface is exposed, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces (e.g. claims 96, 106, 111 and 116), and the second housing portion is exposed at the top surface (e.g. claims 96, 106); and

- a conductive trace (3 and 8) that extends outside the insulative housing, is located between the second housing portion and the chip inside the insulative housing (e.g. claim 111), is spaced from the top surface (e.g. claim 111), includes a top surface that faces away from the chip and contacts the second housing portion inside the insulative housing (e.g. claim 116), includes a bottom surface that faces towards the chip and contacts the second housing portion inside the insulative housing (e.g. claim 116), is spaced from the top and bottom surfaces (e.g. claim 116), extends through one of the peripheral side surfaces (e.g. claim 116) and is electrically connected to the pad inside the insulative housing.

7. Claims 1 - 5, 7 - 13, 15 - 23, 25 - 30, 61, 62, 65, 76, 77, 80, 141 - 143 and 145 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura et al. '809.

a. Nakamura et al. discloses in e.g. Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface (facing the bottom of the page), a lower surface (facing the top of the page) and four outer side surfaces between the upper and lower surfaces (e.g. claims 11, 61, 66, and 71), wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25); and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

b. Regarding e.g. claims 1 - 5, 11, 13, 61 and 62, Nakamura et al. discloses in e.g. Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- an insulative housing (21, 27 and 28) that includes a first single-piece non-transparent insulative housing portion (27) that contacts the chip, covers the lower surface and the side surfaces (e.g. claims 61 and 66), contacts the lower surface and the side surfaces (e.g. claims 2, 11, 62 and 72) and is spaced from the light sensitive cell as well as the upper surface (e.g. claims 3 and 11) and a second transparent insulative housing portion (21 and 28) that contacts the first housing portion, the conductive trace (e.g. claim 4) as well as the light sensitive cell and is spaced from the lower surface (e.g. claims 5, 11 and 61), wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within the peripheral ledge (e.g. claims 1 and 13) and portion (21) is exposed; and

i. Further, regarding the limitation "is spaced from the upper surface" (e.g. claim 11), Nakamura et al. teaches that the chip is pressed into the insulative housing portion (28) prior to the housing being cured (column 1, lines 49 - 63). As such,

even though the figure doesn't depict the spacing, in fact, the insulative housing portion (27) will necessary be spaced from the upper surface of the chip.

ii. Regarding e.g. claims 7, 15, 17 and 25, Nakamura et al. discloses in e.g. Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 the first housing portion being a transfer molded material that includes a peripheral ledge, and the second housing portion being a cured polymeric material that is located within the peripheral ledge and includes a first surface that faces towards the chip and contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that faces away from the chip and provides the central portion of the top surface and is exposed.

iii. Regarding e.g. claims 8 and 18, Nakamura et al. discloses in e.g. Fig. 2 the conductive trace extending through a peripheral side surface of the first housing portion and contacting the second housing portion without extending through a surface of the second housing portion. Furthermore, the term a "surface" reads as at least one surface through which the conductive trace doesn't extend. In Nakamura et al., the conductive trace doesn't extend through at least the top surface.

iv. Regarding e.g. claims 9, 19, 28 and 29, Nakamura et al. discloses in e.g. Fig. 2 the device being devoid of an electrical conductor that extends through opposing surfaces of the second housing portion. The examiner reads the term "electrical conductor" as referring to an additional structure, separate from the conductive trace, because if the term

"electrical conductor" were to read on the "conductive trace", the claim would raise 112-1st new matter issues.

v. Regarding e.g. claims 10, 20, 30, 65, 80 and 145, Nakamura et al. discloses in e.g. Fig. 2, column 9, line 37 and column 10, lines 37 – 47 that bumps 24 are formed by an electric plating method and a ball-bonding method and may be composed of gold. Thus, the device being devoid of wire bonds, TAB leads and solder joints.

vi. Regarding e.g. claim 12, Nakamura et al. discloses in e.g. Fig. 2 the second housing portion including first and second opposing surfaces, the first surface contacts the light sensitive cell and being spaced from the conductive trace, and the second surface faces away from the chip and is exposed.

vii. Regarding e.g. claims 16 and 26, Nakamura et al. discloses in e.g. Fig. 2 the insulative housing consisting of the first and second housing portions.

viii. Regarding e.g. claim 76, Nakamura et al. discloses in e.g. Fig. 2 a conductive trace (22 and 23) that includes a lead (22) and a planar metal trace (23 and e.g. claim 76), wherein the lead extending through an opening in the first housing portion, extending outside the insulative housing and being electrically connected to the pad inside the insulative housing, and the planar metal trace contacting and being not integral with the lead, extending across one of the side surfaces and does not extend outside the insulative housing (e.g. claim 76).

ix. Regarding e.g. claim 77, Nakamura et al. discloses in e.g. Fig. 2 the first housing portion contacting the lower surface and the side surfaces of the chip.

c. Regarding e.g. claims 21, 22 and 23, Nakamura et al. discloses that the device further comprises:

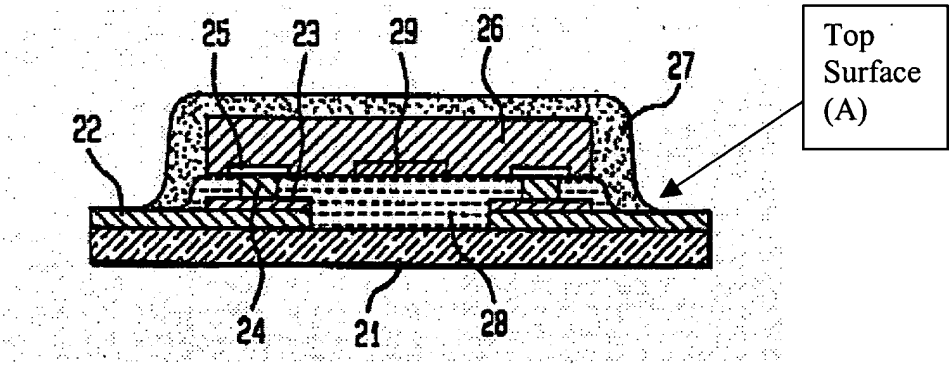
- an insulative housing (21, 27 and 28) that includes a top surface, a bottom surface and uncurved peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first (27) and second (21 and 28) insulative housing portions, the first housing portion is a single-piece that provides the bottom surface, contacts the lower surface and the outer side surfaces (e.g. claim 22), is spaced from the light sensitive cell as well as the upper surface (e.g. claim 22) and is non-transparent, and the second housing portion contacts the upper surface as well as the first housing portion, the light sensitive cell and the conductive trace (e.g. claim 23), is spaced from the lower surface (e.g. claim 23), is farther from the bottom surface than the lower surface is from the bottom surface, provides at least a portion of the top surface and is transparent.

i. Regarding, the limitation "uncurved peripheral side surfaces between the top and bottom surfaces" (e.g. claims 21 and 141), please note that the insulative housing (27) has flat ("uncurved") peripheral side surfaces at least at the center portion of the sides.

ii. Regarding claim 27, Nakamura et al. discloses in e.g. Fig. 2 the light sensitive cell contacting a major surface of the second housing portion that faces towards and being parallel to the upper surface.

d. Regarding e.g. claim 141, Nakamura et al. discloses that the device further comprises:

- an insulative housing (27 and 28) that includes first (27) and second (28) insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface (A), a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion extends into the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip is transparent.




i. Regarding claim 142, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

ii. Regarding claim 143, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 10, 30, 65, 70, 75, 76, 78, 80, 81, 83, 85, 86, 88, 90, 95, 100, 105, 110, 115 and 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Tsuji '282.

Yamanaka discloses the claimed invention except for the device having a planar trace and being devoid of wire bonds, TAB leads and solder joints. However, Tsuji teaches in FIG. 4 and column 3, line 1 - column 4, line 5 a device (8) having a planar trace (10B) that is attached by a bump, that in turn, may be composed of gold (as opposed to solder; column 3, line 9). As such, the device is devoid of wire bonds, TAB leads and solder joints. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Yamanaka by using the planar trace (10B) in the place of bonded wire (8) in Yamanaka, thereby rendering the device devoid the wire bonds, TAB leads and solder joints in the device as taught by Tsuji for at least any of the purposes of (1) avoiding a short circuit that would be caused by contact of the

semiconductor element and the conductive film pattern as taught by Tsuji (column 2, lines 31 - 33); (2) to further reduce vertical height of the package; and (3) to prevent the possibility of wire bonds extending through the upper housing surface.

***Allowable Subject Matter***

10. Claims 31 – 60, 121 – 140 and 146 – 150 are allowed.

11. Claims 14, 64, 67, 69, 72, 74, 79, 82, 84, 87, 89, 92, 94, 97, 99, 102, 104, 107, 109, 112, 114, 117, 119, 120 and 144 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is an examiner's statement of reasons for allowance and indication of allowable subject matter:

a. As was explained above, both Yamanaka '723 and Nakamura et al. '809 teach optoelectronic (OE) semiconductor package devices having first and second housing portions wherein the first housing portion "contacts" the bottom of the chip and at least "covers" the sides of the chip; and wherein the second housing portion is located within the peripheral ledge of the first housing portion. Yamanaka further teaches a device wherein the second housing portion is either recessed relative to the peripheral ledge or is exposed (depending on whether element 91 is interpreted as constituting a further portion of the second housing portion); and the first housing portion forms a portion of the top package surface

and is exposed. Yamanaka does not teach that the first housing portion further contacts (as opposed to covers) the sides of the chip. Nakamura further teaches that first housing portion of that invention contacts the side of the chip, but does not teach that the second housing portion is recessed relative to the peripheral ledge of the first housing, nor that the top of the first housing portion is exposed if transparent substrate 21 is interpreted to constitute part of the second housing portion.

b. However, differing methods were employed to manufacture the respective devices of Yamanaka and Nakamura. For example, Yamanaka disposed the chip within the central, lower recess of the preformed first housing portion such that a gap exists between the sides of the chip and the housing (the first housing covers but does not contact the sides of the chip), and then forms the second housing over the chip within the first housing. Alternatively, Nakamura forms the chip over the second housing portion and then forms the first housing portion over both the chip and the second housing portion, such that the first housing covers and contacts the sides of the chip. As such, the skilled artisan would not have been reasonably motivated to combine some particular aspects/elements of these two respective inventions to arrive at various combinations of limitations that were set forth in particular claims. For example,

i. Regarding e.g., claims 14, 67, 72, 87, 92,97, 102, 112 and 117, the combination of references of does not teach or reasonably suggest the limitation of first housing portion contacting the side surfaces of the chip

in combination with the further limitation that the second housing portion is recessed relative to the peripheral ledge of the first housing portion.

ii. Regarding e.g., claims 31-40, the combination of these references does not teach or reasonably suggest the limitation of first housing portion contacting the side surfaces of the chip in combination with the further limitations that the first housing portion constitutes a peripheral portion of the housing's top surface, and that the second housing portion is exposed.

iii. Regarding claims 121-140 and 146-150, the combination of these references does not teach or reasonably suggest the limitation that a second housing portion does not extend midway between the upper and lower surfaces outside the chip, in combination with either the limitation of (1) the second housing portion being recessed relative to the first housing portion's peripheral ledge (e.g., claim 121) nor (2) the first housing portion being exposed (e.g., claim 126). To clarify the record, the limitation, "does not extend midway," has been interpreted to mean "does not extend at least midway" as opposed to "does not extend only to midway." This is because the former interpretation is consistent with the specification's definition or description of the present invention, whereas the latter interpretation is not.

c. Regarding the limitations relating to a conductive trace having a recessed portion that extends into an insulating housing and a non-recess portion that extends outside of the insulative housing (e.g., claims 41-60, 64, 69, 74, 79, 84, 89, 94, 99, 104, 109, 114, 119 and 144), Glenn et al. '568 teaches such a lead

frame having a partially recessed portion. However, in Glenn the lead is formed at the surface of the package and the recess is incorporated in order to ensure that the lead does not vertically separate from the housing. Since Yamanaka, on the other hand, teaches that the lead 3 is formed so as to be vertically recessed below the upper portion of first housing portion 5, the problem of the lead vertically separating from the first housing portion would not appear to be a problem. As such, absent some potential additional teaching as to why the presence of the lead recess would be beneficial for the Yamanaka device (such as perhaps relating to the structure of the second housing portion), Glenn alone does not provide sufficient motivation for incorporation of this recessed-lead feature.

***Response to Arguments***

13. Applicant's arguments with respect to the claims have been considered and are either partially persuasive or not persuasive for the reasons cited hereinabove or are moot in light of the new grounds of rejection.

***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Webster '219 discloses an image sensor package. See e.g., Fig. 9 wherein the first housing portion 912 contacts the sides of the chip 102s and covers --but does not contact-- the bottom of the chip.

b. Fusaroli et al. '930 discloses an image sensor package (e.g., Fig. 11) that is similar to the Yamanaka device.

c. Glenn et al. '568 (previously made a record) teaches a leadframe having partially undercut leads and die pad in a plastic integrated circuit device package.

d. Osawa JP 6 – 97352 teaches addition conventional processes for attaching a chip to outer leads by means of planar inner leads.

2. **Applicant's amendments filed 5/6/2003 (Amendments B and C, papers #8 and #10) necessitated the new ground(s) of rejection presented in this Office action**. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
12/12/03 2:14:11 PM

BRADLEY BAUMEISTER
PRIMARY EXAMINER

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER